UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,630	08/28/2003	Yasuyuki Doi	60188-640	5559

7590 11/01/2005

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
HOLTON, STEVEN E	
ART UNIT	**PAPER NUMBER**
2673	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,630	DOI ET AL.	
	Examiner	Art Unit	
	Steven E. Holton	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Information Disclosure Statement

3. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. (USPN: 6211849), hereinafter Sasaki in view of Kase (USPN: 5231320).

Regarding claim 1, Sasaki discloses a data driver with "a clock input (Fig. 4, element 2 line labeled CLK), a clock output (Fig. 4, element 3, line labeled CLK), a plurality of data inputs (Fig. 4, element 2 lines labeled DATA), and a plurality of data outputs (Fig. 4, element 3, lines labeled DATA)" which are discussed by Sasaki in col. 4, line 28 – col. 5, line 4). Further, Sasaki discloses a driver circuit with a latching means for latching the plurality of data inputs in synchronization with the clock output and supplying results of the latches as the plurality of data outputs to a display section of the display device (Fig. 4, elements 5 and 7; col. 4, line 46 – col. 5, line 4)". Sasaki also discloses a 'Duty Cycle Regulator' that is used to correct the duty cycle of the clock signal transmitted to the driver circuit (col. 5, line 30 – col. 6, line 27). The 'Duty Cycle Regulator' possesses a 'voltage controlled oscillator (VCO, Fig. 5, element 6c, col. 5 lines 30-55)'. The Examiner notes that 'voltage controlled oscillator possess "a plurality of inverters (Fig. 6, no element labels but each vertical stage of CMOS gates are

inverter circuits; col. 5, lines 42-55)) which are serially connected to each other" and "a second current source connected to a ground side of any one of the plurality of inverters (Fig. 6, the series of CMOS gates connected between the ground and the inverters and controlled with the line labeled 'control voltage'; col. 5, lines 42-55)" and "an end stage inverter of the plurality of inverters supplies the clock output (Fig. 6, element P8 and the line labeled CLOCK OUT; col. 5, lines 42-55)".

However, Sasaki does not expressly disclose 'a first current source connected to a power supply side of any one of the plurality of inverters'; 'wherein a first stage inverter of the plurality of inverters receives the clock input"; "a smoothing circuit for smoothing the clock output to obtain an average voltage"; "a comparator for comparing the average voltage with a reference voltage, wherein if the average voltage is lower than the reference voltage, the comparator supplies a first control voltage to control the magnitude of an electric current in the first current source such that the duty ratio of the cock output increases, and if the average voltage is higher than the reference voltage, the comparator outputs a second control voltage to control the magnitude of an electric current in the second current source such that the duty ratio of the clock output decreases".

Kase discloses a CMOS delay line with a plurality of inverters (Fig. 4, elements Delay 1 – n; more internal structure shown in Fig. 2, col. 2, lines 19-39), a first current source connected to a power supply side of any one of the plurality of inverters (Fig. 4, element VDD is connected to the input power supply side of the inverters as shown in Fig. 2; col. 2, lines 19-39) and, a second current source connected to a ground side of

any one of the plurality of inverters (Fig. 4, element GND is connected to the input ground side of the inverters as shown in Fig. 2; col. 2, lines 19-39), wherein the first stage inverter of the plurality of inverters receives the clock input (Fig. 4, element 31, labeled INPUT; col. 3, lines 60-62), and an end stage inverter of the plurality of inverters supplies the clock output (Fig. 4, element 33, labeled OUTPUT; col. 3, lines 60-62); a smoothing circuit for smoothing the clock output to obtain an average voltage (Fig. 4, element 32, also called a Low Pass Filter (LPF); col. 3, lines 47-51); a comparator for comparing the average voltage with a reference voltage (Fig. 4, element 34, also called a Different Amplifier or D-AMP, the inputs being VX from the LPF and VR (reference voltage) from the voltage divider (Fig. 4, element 36); col. 3, lines 52-59)".

At the time of invention it would have been obvious to one skilled in the art to combine the teachings of Kase and Sasaki to produce a driver circuit for a display system with the ability to correct the duty cycle of an inputted clock signal. The motivation for doing so would have been "to avoid the problems of signal mismatching and narrow output pulses (Kase, col. 1, lines 34-38)" and "to maintain a certain duty cycle range generated by each individual delay inverter (Kase, col. 1, line 39-41)." Thus, it would have been obvious to combine Sasaki and Kase to produce a device as disclosed in claim 1.

Regarding claim 2, Kase discloses, "the first current source is connected to a power supply side of the first inverter (Fig. 4, element VDD, is connected through Fig. 2, element 18 to the power supply side of the first inverter; col. 2, lines 19-39), and the second current source is connected to a ground side of the third inverter (Fig. 4,

element GND, is connected through Fig. 2, element 20 to the ground side of the third inverter; col. 2, lines 19-39)." The Examiner notes that the first and second current sources are connected to the power and ground sides of all of the inverters used by Kase. Also, Kase discloses using 32 delay units row a total of 64 inverters connected in series (col. 3, lines 25-30). The use of fewer or more inverters within the delay line system would be an obvious choice for one skilled in the art.

Regarding claim 3, Kase discloses "the first current source is connected to a power supply side of the first inverter (Fig. 4, element VDD, is connected through Fig. 2, element 18 to the power supply side of the first inverter; col. 2, lines 19-39), and the second current source is connected to the ground side of the first inverter (Fig. 4, element GND is connected through Fig. 2, element 20 to the ground side of the first inverter; col. 2, lines 19-39)." As stated above regarding the rejection of claim 2, it would have been obvious to one skilled in the art to change the number of inverters in the delay line system.

Regarding claim 6, Sasaki discloses, "further comprising level shift means for increasing a small amplitude of each of the clock input and the plurality of data inputs to a predetermined level inside the data driver (Fig. 4, element 4; col. 4, line 46 - col. 5, line 4)."

Regarding claim 7, the Examiner notes that it would have been obvious to on skilled in the art that by changing the level of the voltage signal VR of Kase by selecting different values for the resistors R1 and R2 shown in Fig. 4; col. 5, lines 56-59, the voltage level of the reference voltage supplied to the comparator could be altered.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of Kase as applied to claim 1 above, and further in view of Murata et al. (USPN: 6144355), hereinafter Murata.

Regarding claim 4, as shown above the combination of Sasaki and Kase disclose all of the limitations of claim 4 except, "further comprising a plurality of data inverter chains between the plurality of data inputs and the latching means, wherein each of the plurality of data inverter chains has the same internal structure as that of the inverter chain that supplies the clock output, and in each data inverter chain, an electric current control is performed based on the first and second control voltages."

Murata discloses a driver circuit system with a clock control circuit performed on the clock and data input lines before the first latching circuit (Fig. 6, elements 34 are the clock control circuits discussed in col. 7, line 64 – col. 8, line 48 with reference to Figs. 9 and 10)."

At the time of the invention it would have been obvious to one skilled in the art that the input lines for data and clock for the drivers made by Sasaki could further have the PLL or clock correction circuits added to the input lines for data as shown by Murata. This would have been a design choice in light of the teachings of Murata who shows systems with and without the PLL devices on the data input lines (Figs. 5 and 6 respectively; col. 7, lines 48-62). Thus, it would have been obvious to one skilled in the art to combine the teachings of Sasaki, Kase, and Murata to produce a device a specified in claim 4.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of Kase as applied to claim 1 above, and further in view of Hirabayashi (USPN: 6469557).

Regarding claim 5, as discussed above, the combination of Sasaki and Kase disclose all of the limitations of claim 5 except, "a first auxiliary current source connected in parallel to the first current source, and a second auxiliary current source connected in parallel to the second current source; and the first and second auxiliary current sources are not controlled based on the first or second control voltage".

Hirabayashi discloses a delayed clock signal generation circuit that is a series of inverters connected in series to the clock cycle. Hirabayashi further discloses first current and second current sources that are connected by to a control signal to alter the current source provided to the power and ground sides of the inverters (Fig. 2, elements Q5 and Q6 provide the sources that are altered by control signals; col. 4, lines 1 – 27). Hirabayashi also discloses the 'auxiliary sources' that provide constant levels to the power and ground sides of the inverters (Fig. 2, elements Q1 and Q4 (not labeled within the figure but the unlabeled CMOS gate within a single inverter); col. 4, lines 1-27).

At the time of invention it would have been obvious to one skilled in the art to combine the parallel source system of Hirabayashi with to the delay circuit of Kase. The motivation for doing so would have been "to provide a semiconductor integrated circuit and a delayed clock signal generation method capable of simply and rapidly adjusting a delay time of a delayed clock signal in accordance with a change in frequency of an

input clock signal (Hirabayashi, col. 2, lines 8-13)." Thus, it would have been obvious to combine the teachings of Sasaki, Kase and Hirabayashi to produce the device as specified in claim 5.

Conclusion

7. The Examiner notes that the terms used by the applicant are non-standard in describing some of the electrical circuitry described within the invention. The inverter chain is also known as a 'voltage controlled oscillator', 'ring oscillator', and 'delay line', and the smoothing circuit is more commonly known as a 'low pass filter'.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven E. Holton whose telephone number is (571) 272-7903. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven E. Holton
October 30, 2005
Art Unit 2673

VIJAY SHANKAR
PRIMARY EXAMINER